**Ibrahim**

**Rupawala**

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**San Jose**

**95132**

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[**ibrahimrupawala@gmail.com**](mailto:ibrahimrupawala@gmail.com)

**Arizona State University**

**Tempe, AZ**

**Electrical & Electronics**

**3.74/ 4**

**01/2016**

**12/2017**

**Gujarat Tech University**

**Milpitas, CA**

**Electronics**

**8.27/10**

**07/2009**

**05/2013**

**Oscilloscope**

**Logic Analyzer**

**Probe Station**

**Device Characterization**

**Semiconductor Device Physics**

**ASIC Design**

**Data Processing**

**Data Parsing**

**Object Oriented Programming**

**Python**

**HSPICE**

**Scripting**

**RTL Design**

**Static Timing Analysis**

**TCL**

**Verilog**

**System Verilog**

**C/ C++**

**www.linkedin.com/in/irupawala**

**Ibrahim Rupawala**

**Staff Electronics Engineer**

**Western Digital Inc**

**951 Sandisk Dr**

**Milpitas, CA**

**95132**

***01/2018***

\* Responsible towards various aspects of 3D NAND flash memory chip design, focusing on Micro Architecture, RTL, Logic synthesis, gate level simulation and equivalence checking to deliver target power, performance and area goals.

\* Performed feasibility studies at the beginning of design phase for new architecture and features.

\* Performed post-silicon electrical and physical failure analyses to debug the design and identify the root cause for functional and parametric yield losses reported by external and internal product lines using lab tools.

\* Implemented changes as part of ECO (Engr Change Order) for bugs and improvement items in synthesized modules.

\* Validated and optimized multiple design and device modes using lab tools to ensure the functionality and product specifications like power consumption, performance, energy per bit, bit error rate, etc are met.

\* Designed multiple trims to optimize NAND Flash device specifications (endurance, performance, power) as per the requirement of business units. Developed tests, patterns/vectors, timing, and diagnostics on company’s proprietary ATE’s.

\* Developed multiple screens and monitors to ensure the health of the dies and meet the yield criteria (DPPM).

\* Debugging issues, weak points, or potential improvement areas related to any portion of the System Level Tests (SLT’s) to help facilitate system features and to improve system level performance and reliability to meet customer specifications.

**Product Engineering Intern**

**Micron Technology Inc**

**110 Holger Way**

**San Jose, CA**

**95134**

**05/2017**

**12/2017**

\* Optimized the erase/program/read timings and voltages parameters to configure the power and performance of the chip.

\* Designed silicon test plan and correlated silicon to simulation data. Performed post-silicon validation to validate design.

\* Design of Experiments (DOE) to collect data using company’s ATE’s to provide estimation for product life, performance, reliability and to predict failure modes. Documented results and communicated to respective stake holders.

\* Developed scripts to automate characterization, verification and simulation flows and reduce the test time.

\* Documented the design specifications, behavioral description, and timing diagrams.

**Graduate Teaching Assistant**

**Arizona State University**

**1151 S Forest Ave**

**Tempe, AZ**

**85281**

**10/2016**

**05/2017**

\* Helped students in performing lab assignments using cadence environment for the course Analog & Digital Circuits.

**IC Design Intern**

**Analog Rails**

**3615 S. Jojoba Way**

**85248**

**Chandler, AZ**

**05/2016**

**07/2016**

\* Designed standard cell library and performed characterization of the cells. Performed RTL verification of the cells.

\* Characterized standard cell library creating models for delay, function, constraints and power that efficiently model cell behavior. Developed the Layout of standard cells in 45 nm PDK and performed DRC and LVS checks.